# Digital Analog Converter for the Extraction of Test Signals from Mixed Integrated Circuits

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**Abstract.** The construction of integrated circuits involves testing the correct operation of its internal blocks. For this, a common practice is the integration of functional blocks to stimulate the internal subsystems and extract the responses to those stimuli. In this article, the design and simulation of a circuit for the extraction of the response signals of the devices under test in analog and mixed-signal integrated circuits is presented. The extraction block is a 2-stage 5-bit segmented A/D converter, operating at a sampling frequency of 10 MHz, implemented in a 0.12 μm technological process, which can be powered with 1.5 Vdc. This proposal offers a reduction in the area consumed, by requiring fewer comparators than other similar solutions found in the literature.

**Keywords:** Digital analog converter · Signals · Mixed integrated circuits

## 1 Introduction

The combination of the growing demand for consumer electronics and the constant growth in the packaging density of semiconductor devices, is leading to the integration of more and more functional systems into a single integrated circuit [1]. The result, among other things, is an increased need for the integration of analog and mixed-mode components, e.g. analog-digital, RF-analog-digital, and mechanical-analog-digital, into the same chip or package [17]. Designing such SoC (Systems on Chip) is undoubtedly a challenge, since it links abstraction management at the system level while simultaneously dealing with the physical effects of transistors and the parasitic effects associated with the circuit [2]. Similarly, the next generation of SoC testing represents a real challenge, especially when cost and time to market are usually key requirements. Such mixed-signal integrated circuits contain very complex signal paths and functional specifications, and the test programs developed may not be very viable, as they would be significantly slow

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O. Gervasi et al. (Eds.): ICCSA 2021, LNCS 12949, pp. 207–223, 2021.
https://doi.org/10.1007/978-3-030-86653-2_15

in characterizing and debugging the device, which would greatly increase the time to market [2, 28]. The difficulty is accentuated by another aspect of system-level integration, called third- party functional block integration. In order to compete with the complexity of design, the manufacturers of the final system are forced to rely on pre-designed blocks, and carry out the integration of these as part of a larger and more complex system. These functional blocks are obtained from virtual libraries that use software to describe the block as part of the system [3, 7].

In the digital domain, the test mechanisms and techniques are capable of testing most devices in this domain, and the test information can be transported seamlessly throughout the SoC [8–11]. The results can also be extracted in the same way. For this reason, it seems possible to derive a systematic procedure by which the integrator of the final system can access the virtual functional blocks that make up the chip. The problem in the analog domain is how complicated it is to extract test signals over long interconnect lines inside a chip. Rapid degradation of the signals is very likely due to noise and distortion introduced by the parasitic behaviour of some elements within the integrated circuit [4–6].

One of the problems to which an alternative solution is sought is the case of ICs containing analogue functional blocks, and the aim is to test the functioning of these blocks. Test signals from such blocks must travel inside the chip and then be extracted. As is well known, analogue signals are very sensitive to interference, are not immune to noise, and degrade more easily than digital signals [9, 16, 17]. Therefore, the tests on this type of block are not very reliable, since both the input and output signals are disturbed by noise and do not reveal the true behaviour of the block. This problem is compounded by the fact that, at high frequencies, the microband or interconnection lines of each of the elements that make up the system begin to behave like transmission lines, and the following manifestations appear: energy reflection, attenuation, impedance decoupling both at the source and at the load relative to the interconnection line [9, 17]. As a result, manufacturers must perform impedance couplings, source and load balancing, among many other procedures to solve the above mentioned problems. These solutions require design times that manufacturers are not willing to take [2].

Due to the above, one objective of these test techniques is the integration of this block into the chip to be tested, which would pose a problem due to the difficulty associated with the transport of analog signals on an integrated circuit, in particular the fact that these types of signals are very sensitive to noise and the tests could be affected and not show the results that show the real behaviour of the circuit [12–15, 32]. Methods based on the inclusion of data converters, such as D/A and A/D converters, have been presented in the industry as alternatives [4, 5, 27]. The first one for obtaining analog waveforms from digital words, and the second one for extracting in digital format the output signals of the blocks under test, CUT (Core Under Test). For the above, it is clear that the use of D/A converters would be prohibitive, due to the excessive use of area in the silicon tablet, considering that the latter is a critical requirement in the design of VLSI integrated circuits [1]. The aforementioned techniques are static, consisting of predesigned fixed blocks. This has evolved to dynamic solutions based on adaptive [29] and intelligent techniques [30, 31].

The resolution of the waveform digitizer shall be 5 bits and the sampling frequency shall be 10 MHz. The technology for which the circuit proposed here was designed is a 0.12 μm CMOS lithographic process. This process is characterized by having a power level of between 1 V and 1.5 V, and it is assumed that the integrated circuits where this test block is assembled can provide them, since they turn out to be typical of this technology [26]. On the other hand, the dual levels of these voltages are required, these are −1 V and −1.5 V. As the circuit designed in this project is to be used in mixed integrated circuit tests, it is to be assumed that they are also provided by the chip. Other features that characterize this technology are its threshold voltage, V_t, which is around 0.3 V, and an oxide layer thickness of 4 nm.

## 2 Analogical – Digital Conversion Process

Signal A/D conversion is done in 2 stages, the first is uniform time sampling and the second is amplitude quantization. The samples x[n], evenly spaced time intervals Ts, of the continuous time signal x(t), can be represented by x[n] = x (nTs). In the frequency domain, the sampling process produces periodically repeated versions of the original signal spectrum placed in the integer multiples of the sampling frequency fs = 1/Ts. The above is evidenced in Eq. (1), where Xs (f) represents the spectrum of the sampled signal, and X (f) is the spectrum of the original signal in continuous time [18].

$$Xs(f) = \frac{1}{Ts} \sum_{k=-\infty}^{\infty} X(f - kfs) \tag{1}$$

This process is shown in Fig. 1, for the case where fs = 2W, where W is the highest frequency component of the original signal. In general, the continuous-time signal can be reconstructed from its samples, if repeated versions of the spectrum do not overlap. To achieve the above, the original signal should be band-limited to half the sampling frequency [19].

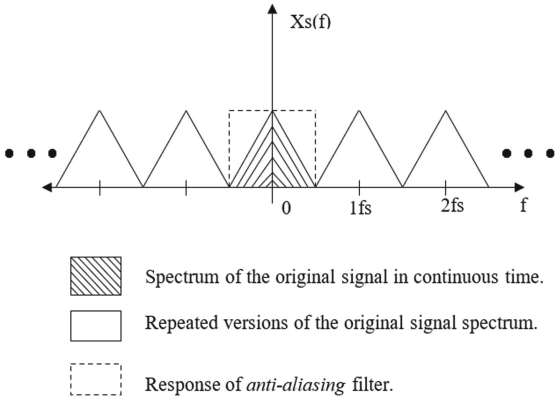


**Fig. 1.** Shape of the power spectrum of a sampled signal.

The overlap between repeated versions of the signal spectrum is known as aliasing, the aliasing does not allow the reconstruction of the signal from its samples. An anti-aliasing filter is regularly used to ensure this requirement [20]. The anti-aliasing filter is an analog low-pass filter that precedes the sampling circuit. The case where the sampling frequency is fs = 2W, is known as Nyquist rate sampling, and is considered critical because that the anti-aliasing filter must have a frequency response with a small transition band [19].

The sampling process is an invertible operation because there is no loss of information. Note that although Fig. 1 shows the sampling process for a baseband signal, Eq. (1) describes the sampled spectrum for any signal spectrum centered on some frequency component other than 0, fc. Assuming the signal has a bandwidth W, the spectrum of the original signal comprises the range [f_c − W/2, f_c + W/2]. To avoid aliasing some authors suggest sampling at rates f_s ≥ 2W [19].

Once the sampling is done, a process called quantization follows. This process involves approximating the values of the samples to a finite set of values, using a closeness criterion. In this stage the dynamic range of the input signal is divided into equal parts, for uniform quantization. A representative value is assigned to each sector. Samples are assigned one of these values, depending on the sector where it is located. The typical transfer characteristics of A/D Quantizers or Converters are shown in Fig. 2 [19].

Quantization is a non-reversible process. Quantified output amplitudes are usually represented by digital code words with a finite number of bits. For example, for a 1-bit A/D converter as shown in Fig. 2(c), the output values V and −V can be mapped to the digital codes “1” and “0.” Another way to visualize this is by using the digital code words instead of the output values on the axis and in Fig. 2. Quantified output values can be considered as the ideal A/D converter output, whose output corresponds to a digit code word [19].

An A/D converter or quantifier with Q output levels is said to have a resolution of N bits if N = ΔlogΔ_2 (Q). It should be made clear from Fig. 2 that for an A/D quantifier or converter of Q levels of quantization, only input values separated by at least a distance Δ = 2V/(Q − 1) can be distinguished or designated for different output levels. N bits are required to encode the corresponding Q code words with each output level.

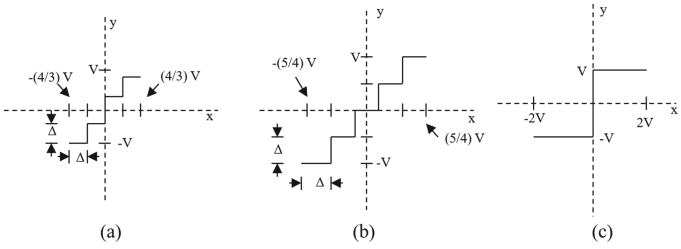


**Fig. 2.** Transfer characteristics of typical quantifiers.

The transfer curves of the quantifiers in Figs. 2(a) and (b), which are symmetrical, will now be exalted. The half-increase quantifiers do not have an output level of 0 for an input value of 0, generating a DC offset undesirable, as seen in Fig. 2(a). The half-step

quantifier, Fig. 2(b), needs an even number of output levels to produce a completely symmetrical transfer curve. This is an advantage because the number of output levels could be a power of 2 and be encoded exactly with $N = log_2 (Q)$ bits. On the other hand, the half-step quantifier needs an odd number of output levels, making Q not a power of two and therefore no efficient coding is performed. For this case, the number of bits needed could be $N = log_2 (Q - 1) + 1$, where $Q - 1$ is taken as a power of 2.

If the number of output levels of the half-step quantifiers are forced to be powers of 2 to use only Q − 1 levels, there will be a large amplitude distortion. The distortion, of course, could be negligible when the number of output levels is large.

Most A/D converters provide trade-offs between signal bandwidth, output resolution, and complexity of digital and analog hardware. The qualitative compromises between resolution and band width of some of these techniques are shown in Fig. 3.

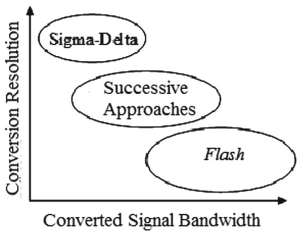


**Fig. 3.** Commitment resolution vs. bandwidth.

The quantifier used in any A/D converter is a non-linear system, which makes analysis difficult. To make the analysis manageable, the quantifier is usually made a linear system and modeled through a noise source, e[n], added to the signal x[n], to produce the quantified output signal y[n]:

$$y[n] = e[n] + x[n] \tag{2}$$

The block diagram of the model of an A/D converter system displaying the sampling process and the quantifier is shown in Fig. 4. In addition, to simplify the noise analysis of the quantifier.

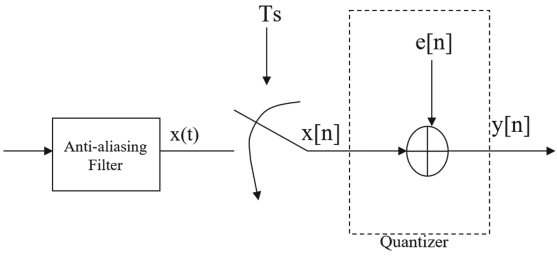


**Fig. 4.** Block diagram and model of a conventional A/D converter.

## 3 Convertering Circuits A/D

These are the electronic circuits responsible for carrying out the quantification of the samples obtained from the analogue signal. There are different types of A/D converters, the usefulness of which will depend on the characteristics of the conversion applications [17, 21].

### 3.1 Flash A/D Converters

The architecture of this converter consists of a string of comparators, which have their inputs connected to a resistance ladder, and their output is fed into a digital encoder circuit, which gives a binary value representative of the highest level of comparison exceeded. It is possible to minimise the quantification error by selecting the values of the resistances at the ends of the chain in an appropriate way [21].

### 3.2 Successive Approaches

There they are circuits that use as one of their constitutive blocks a D/A converter in a feedback architecture. They deliver an output of n bits in n clock cycles, making successive comparisons of the input with the output of a D/A converter, and dividing the range in half in each cycle, this is achieved by varying from bit to bit, from the most to the least significant [22].

### 3.3 Converters to Ramp and Double Ramp

The single ramp structure is prone to errors caused by variations in components, particularly the capacitor, and to deviations in the frequency of the oscillating circuit. Therefore, double ramp architectures are much more used, where such errors are compensated by means of a double integration. In the first ramp, the capacitor voltage starts at zero and is charged for a fixed time to a current that depends on the input voltage. Then, in a second phase, it is discharged at constant current for a time which is measured by a meter [23].

## 4 Proposed Signal Digitalizer

The A/D converter, two-stage ADC, has a conventional Flash A/D converter at its heart. The latter has as constitutive circuits the operational amplifier and the comparator, as well as a convenient logic. A diagram of how the digitizer block is structured can be seen in Fig. 5.

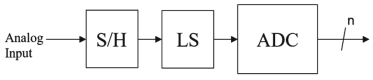


**Fig. 5.** Block diagram of the signal digitizer

### 4.1 ADC Block

Alternatives were presented only in the A/D conversion section. Three alternatives were considered, namely. The first was an A/D converter of successive approximations, or SAR, but it was very slow, consuming as many clock pulses as bits of resolution it had. In the case of 5 bits, it would be 5 clock strokes. It was discarded for speed reasons. The second option was a conventional Flash A/D converter, but its area consumption turned out to be excessive and therefore prohibitive for this application. The last consideration, which was the one chosen, is the 2-stage Flash A/D converter. Consumption of small area, similar to that of one of successive approaches, but with the speed of a conventional Flash [24] (Fig. 6).

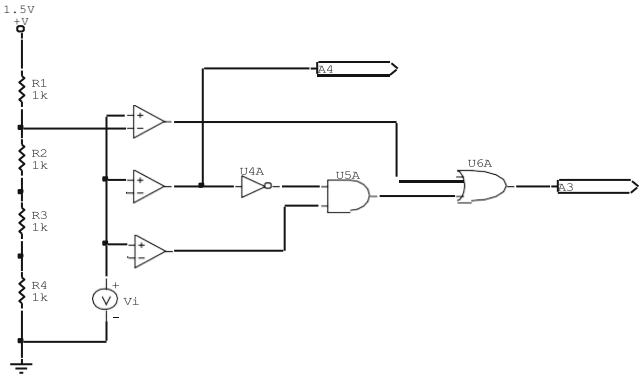


**Fig. 6.** 2-bit Flash converter.

In this design it has been assumed that the dynamic range of the signal is between 1.5 V and 0 V, in case of a change in the signal range, only the voltage in the resistive network generating the references should be changed. In this project, a standard 1 kΩ resistor type has been used, to facilitate manufacturing in an integrated circuit. The function of this first block is to divide the dynamic range of the signal into four equal sectors, and the 2-bit code on the output will indicate which of the four regions the input sample is in. Table 1 shows this operation.

**Table 1.** Divide the 2-bit A/D converter into four sectors.

| Voltage of analogue in. | A4 | A3 | Area |
|---|---|---|---|
| 0 V < Vin < 0.375 V | 0 | 0 | 1 |
| 0.375 V < Vin < 0.75 V | 0 | 1 | 2 |
| 0.75 V < Vin < 1.125 V | 1 | 0 | 3 |
| 1.125 V < Vin < 1.5 V | 1 | 1 | 4 |

This way you get the 2 most significant bits. The comparator used in this section is based on an operational amplifier presented in a previous article [25].

Once the first two bits have been obtained, the sample is taken and pre-processed before obtaining the remaining three bits. The first is to use a D/A converter to transform the two bits already obtained into an analog voltage, a standard configuration for this block called a ladder network is used, and shown in Fig. 7.

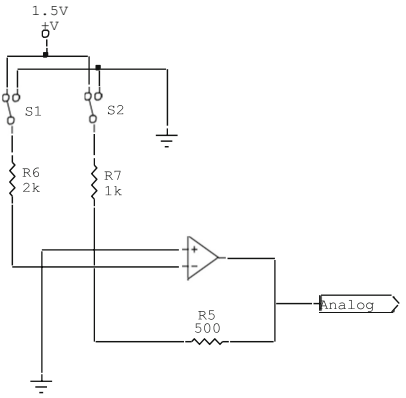


**Fig. 7.** 2-bit D/A converter.

There is an equation that governs the operation of this circuit, and that was the basis for the elaboration of the design, this is shown below

$$V_o = \frac{-V_{ref} \cdot R5}{R7}(2^1 \cdot B1 + 2^0 \cdot B0) \tag{3}$$

In this equation $V_{ref}$ is the supply voltage, which for this case is 1.5 V, R5 is the feedback resistor, which for this application is 500 Ω, and R7 is the resistor corresponding to the most significant bit, which in the circuit used here has a value of 1 kΩ. The switches S1 and S2 are controlled by the 2 bits already obtained previously, and corresponding to A0 and A1 respectively. The operation of the circuit is shown in Table 2.

**Table 2.** Input Output ratio of the 2-bit D/A converter.

| A1 | A0 | Output voltage (V) | Area |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | −0.375 | 2 |
| 1 | 0 | −0.75 | 3 |
| 1 | 1 | −1.125 | 4 |

From this table and from Eq. (3) we can deduce the following conclusions: when A0 is active, 0.375 V must be added, and when A1 is active, 0.75 V must be added, therefore it can be concluded that

$$\frac{V_{ref} \cdot R5}{R7} = 0.375 \text{ V} \quad (9.18)$$

If you have to $V_{ref} = 1.5$ V, R7 = 1 kΩ, then we get that R5 is 500 Ω, just like we said, getting the circuit in Fig. 7.

The next step is to subtract the analog value obtained previously from the sample value, and to the result of this subtraction apply a conventional 3-bit A/D converter type Flash, and in this way you get the 3 least significant bits, and generally a 5-bit code. Because the analogue levels at the output of the D/A converter are inverted, not a subtractor circuit is used but a summator. The latter process is equivalent to dividing the four zones described above into 8 sub-zones each, and determining the location of the sample related to these sub-zones. The sample summing circuit in Fig. 8.

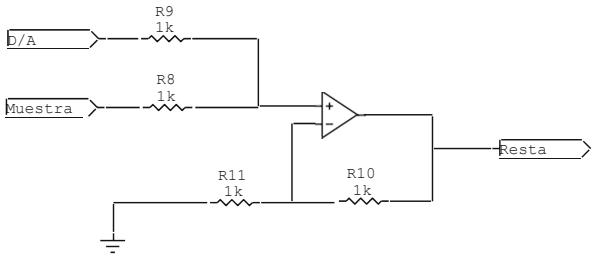


**Fig. 8.** Remaining circuit.

For this block, as well as for the D/A converter, the operational amplifier designed and presented in a previous article is used [25].

The next step, the one that proceeds to the subtraction, is a 3-bit Flash converter. The converter implemented here is divided into two parts, the first is a comparison circuit, which consists of a series of 7 comparators and a reference generator circuit and can be seen in Fig. 9. The second part is a coding block, which takes the thermometer-type outputs of the comparators and transforms them into a 3-bit binary code, its architecture can be seen in Fig. 10.

### 4.2 LS Block

It is the first part of the signal digitizer, and is responsible for adding an offset level to the signal coming from the block under test. The aim of this is to ensure that there are no changes in polarity in the signal that is to be digitized, and thus to make the design of the A/D converter more flexible, which will be described later. A summing block was used, which is based on the voltage summing configuration of the operational amplifier. The level slider scheme is shown in Fig. 10. As can be seen in the figure, the added offset voltage is 0.75 V, assuming that the output signal of the block under test does

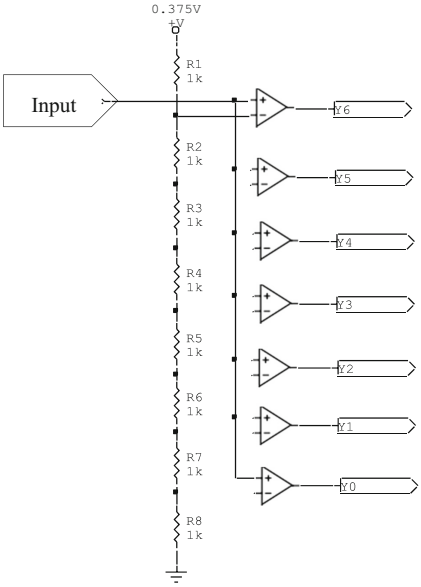


**Fig. 9.** 3-bit Flash A/D converter.

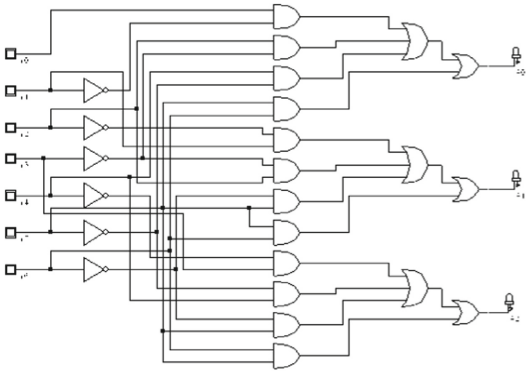

**Fig. 10.** 3-bit thermometer output encoder.

not exceed 1 V peak to peak. This value may change depending on the application in question. Resistances R3 and R4 must be of the same value for the following ratio to be met:

$$V_o = \left(1 + \frac{R7}{R1}\right)\left(\frac{V_i + 0.75V}{2}\right)$$

Immediately you can see that R7 must be equal to R1, if you want the voltage at the output to be the sum of the input voltages.

### 4.3 S/H Block

The sam pling frequency was 10 MHz as specified, but for technical reasons it is not possible to sample at this frequency, therefore it was decided to lower the rate to 5 MHz, once seen the results will be concluded because such a change had to be made. This implementation offers a compact and practical solution, especially contributing significantly to space savings, making it ideal for integrated applications. This circuit has only one drawback, and it is the fact that the value of the sample changes during the whole high level of the clock pulse, a fact that was thought not to represent problems in this project, because as a Flash converter is used, the codes are generated almost instantly, and the code corresponding to the last value that I took the sample during the cycle will be captured. clock. However, the latter is not true, as it takes the A/D converter a while to stabilize the output code. When the simulations and tests were performed, it was found that the use of this type of single circuit was not suitable for the purposes of the work. This could be solved with the inclusion of an isolation circuit, in this case, it was an operational amplifier connected as a buffer or follower. The result is the circuit shown in Fig. 11. These above-mentioned situations will be further clarified in the chapter on tests and results.

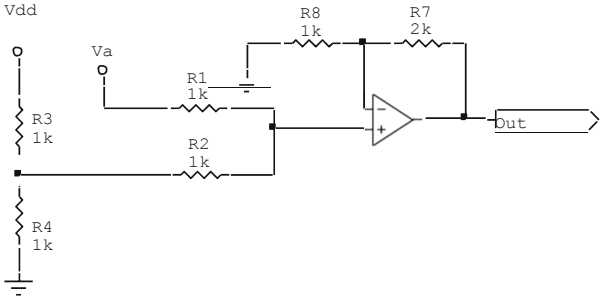


**Fig. 11.** Level shifter circuit.

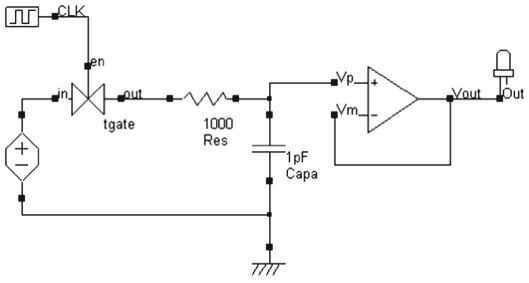


**Fig. 12.** Sampling and maintenance circuit.

## 5 Results Overalled

The operation of the signal digitizer is summarized in Table 3, which shows that each range of the input signal corresponds to a binary code. So, what we should expect is that for every sample taken within a given range, we get the corresponding binary code at the encoder output. As can be seen, the static tests of the converter were satisfactory, as all codes were correctly assigned to the corresponding sample. But it should be noted that the simulations showed that it took the converter some time to find the correct code corresponding to the input sample. This time was called the set-up time, and was measured for each test. See Table 4. The ramp sign is shown in Fig. 12. The output codes are shown in Fig. 13. In this last figure it is possible to notice that there is a behavior in time of the countdown type, which corresponds to a ramp type input, which increases its value gradually. The figure shows the codes that are loaded into the log over time.

**Table 3.** Operation summary of the 5-bit A/D converter.

| Voltage ranges | Binary code | Area |
|---|---|---|
| 0 V–0.047 V | 00000 | 1 |
| 0.047 V–0.093 V | 00001 | 2 |
| 0.093 V–0.14 V | 00010 | 3 |
| 0.14 V–0.187 V | 00011 | 4 |
| 0.187 V–0.234 V | 00100 | 5 |
| 0.234 V–0.281 V | 00101 | 6 |
| 0.281 V–0.328 V | 00110 | 7 |
| 0.328 V–0.375 V | 00111 | 8 |
| 0.375 V–0.422 V | 01000 | 9 |
| 0.422 V–0.469 V | 01001 | 10 |
| 0.469 V–0.516 V | 01010 | 11 |
| 0.516 V–0.563 V | 01011 | 12 |
| 0.563 V–0.61 V | 01100 | 13 |
| 0.61 V–0.657 V | 01101 | 14 |
| 0.657 V–0.704 V | 01110 | 15 |
| 0.704 V–0.751 V | 01111 | 16 |
| 0.751 V–0.798 V | 10000 | 17 |
| 0.798 V–0.845 V | 10001 | 18 |
| 0.845 V–0.892 V | 10010 | 19 |
| 0.892 V–0.939 V | 10011 | 20 |

(*continued*)

**Table 3.** (*continued*)

| Voltage ranges | Binary code | Area |
|---|---|---|
| 0.939 V–0.986 V | 10100 | 21 |
| 0.986 V–1.033 V | 10101 | 22 |
| 1.033 V–1.08 V | 10110 | 23 |
| 1.08 V–1.127 V | 10111 | 24 |
| 1.127 V–1.174 V | 11000 | 25 |
| 1.174 V–1.221 V | 11001 | 26 |
| 1.221 V–1.268 V | 11010 | 27 |
| 1.268 V–1.315 V | 11011 | 28 |
| 1.315 V–1.362 V | 11100 | 29 |
| 1.362 V–1.409 V | 11101 | 30 |
| 1.409 V–1.456 V | 11110 | 31 |
| 1.456 V–1.5 V | 11111 | 32 |

**Table 4.** Results of static tests of the A/D converter.

| Test sample | Code obtained | Binary code | Status | Area | Error (V) | Error (%) | Time of establishment (ns) |
|---|---|---|---|---|---|---|---|
| 1.48 V | 11111 | 11111 | Correct | 32 | 0 | 0 | 10 |
| 1.43 V | 11110 | 11110 | Correct | 31 | 0 | 0 | 99 |
| 0.54 V | 01011 | 01011 | Correct | 12 | 0 | 0 | 77.55 |
| 0.48 V | 01010 | 01010 | Correct | 11 | 0 | 0 | 62.97 |

A final dynamic test was carried out, which consisted of the input of a sinusoidal wave through the sampling circuit. The input wave had 0.5 V peak, an offset level of 0.75, and a frequency of 500 kHz. All sample values were measured at the points where the signal was captured by the converter output log, and it was checked whether the assigned codes were the Corrects. The simulation time used was 5 μs. The results obtained are shown in Figs. 14 and 15, as well as in Table 5 (Fig. 16).

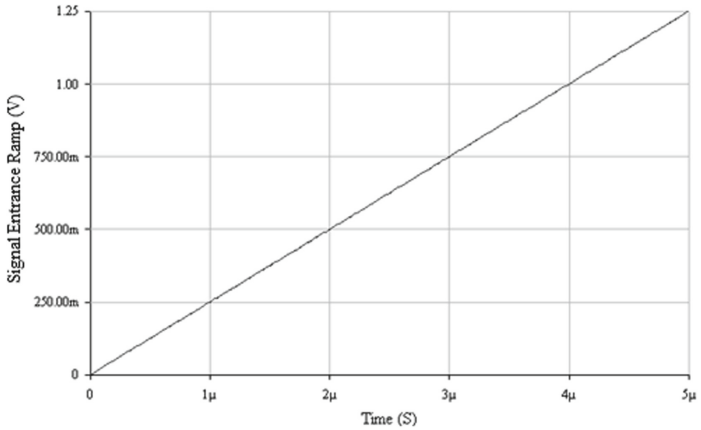


**Fig. 13.** Signal Entrance Ramp.

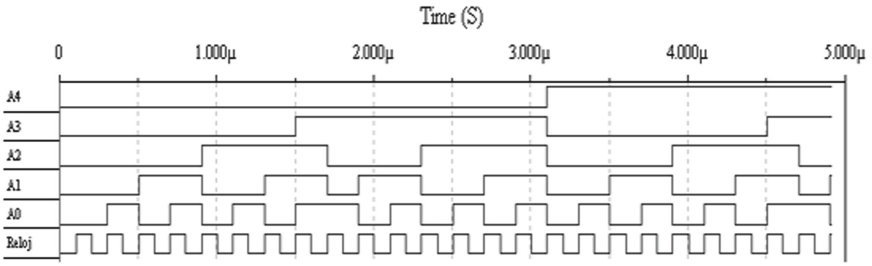


**Fig. 14.** Output of the A/D converter at a ramp input after being loaded.

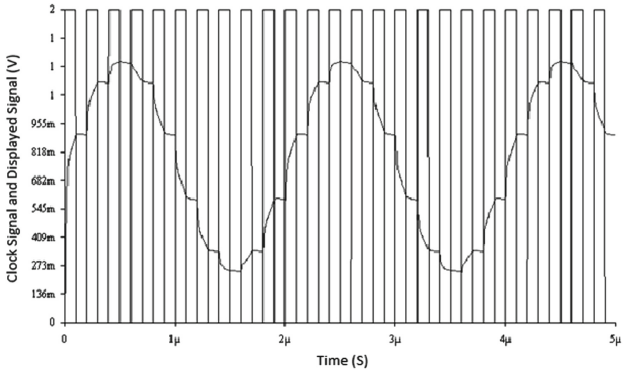


**Fig. 15.** Output signal from the sampling circuit.

**Table 5.** Summary of samples taken during the dynamic test of the A/D converter.

| Sampling time (ns) | Value of the samples (V) | Code obtained | Binary code | Status | Error (V) | Error (%) |
|---|---|---|---|---|---|---|
| 197 | 0.89 | 10011 | 10010 | Error | 0.046 | 3.12 |
| 1395 | 0.33 | 00111 | 00111 | Correct | 0 | 0 |
| 1600 | 0.24 | 00101 | 00101 | Correct | 0 | 0 |

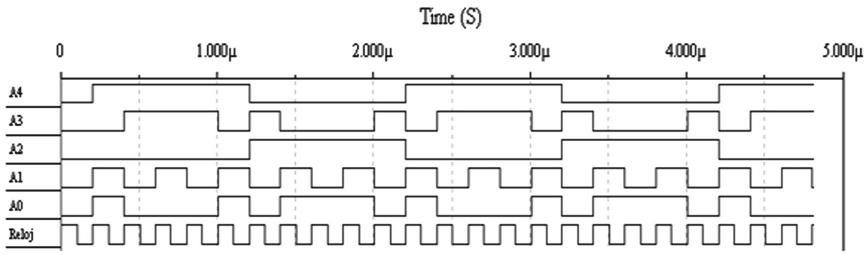


**Fig. 16.** Waveforms of the output bits of the A/D converter before a sinusoidal input.

Correct performance of the A/D converter is remarkable, and one additional comment can be added, the only sample that gave incorrect results was 0.89 V, but there is a reason for this behavior. If we look at Table 3, we see that the code for zone 19, which is where the 0.89 V sample should be, is 10 010, and the limits of this zone are 0.845 V–0.892 V. Zone 20, which code is 10 011 and is the one assigned to the sample under study, has limits 0.892 V–0.939 V. These errors can occur for several reasons. The first is that the determined limits present some problem and are not in agreement with the reality of the circuit. The other possibility is a problem of numerical approxi mation of the software since the difference separating the sample from one region to another is 0.002, which could result in the error found. If these observations are true, the signal digitizer can be said to have achieved the objective.

## 6 Conclusions

The signal digitizer was made under the concept of a 2-stage Flash converter. The maximum resolution achieved without significantly increasing the complexity of the hardware was 5 bits. The time of establishment forced a decrease in the sampling frequency, but, even so, the captured signals had an acceptable quality. The use of this architecture led to a noticeable decrease in the use of comparison devices, compared to the conventional Flash conversion technique, as well as an uncomplex operation, which simplifies the design, compared to SAR conversion techniques. This approach is similar to that presented in [32]. In that paper, a signal extraction block is presented using an 8-bit segmented A/D converter with 2 flash-type stages of 4 bits each. Also, it has a 4-bit D/A converter to perform segmentation. The sampling frequency of that converter is 1.7 MHz, unlike the one presented in this paper, which is 10 MHz. The technological

process of that approximation is 0.5 μm, which establishes its supply voltage at 4 V, while the one presented here has a 0.12 μm process, which reduced the supply voltage to 1.5 V. This reduced voltage limited the range dynamic of the signal to extract, and allowing to use fewer bits.

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